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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/466,180	CAMERON ET AL.	
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-12 and 14-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14* is/are allowed.

6)☒ Claim(s) *16-19,21-23 and 26-28* is/are rejected.

7)☒ Claim(s) *20,24,25,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

2. Claims 1, 3-4, 6-12, and 14-30 are presented for examination. Claims 2, 5, and 13 have been canceled.

3. The abstract of the disclosure is objected to because page 1, line 6 "120" should be –119(e)--. Correction is required. See MPEP § 608.01(b).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 21, 23, 26, and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Watkins, U.S. patent No. 5,937,436.

As per claim 21, Watkins shows a method, comprising:

Storing, in a cache of an adapter installed in a host system (e.g., fig. 4, el. 450 is a cache for storing frequent used address translations, col. 2, lines 14-22; col. 1, lines

54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65;fig. 3, el. 260k is an adapter which joins a switch to bus 270, fig.2A, a workstation 200 is a host system because it is a computer connected to a network or work station 200,CPU 210 controls the attached peripheral devices 260, col. 3, lines 34-38 and col. 4, lines 50-60) and provided to interface a switch fabric (e.g., fig. 3, an ATM Switch and network; col. 3, lines 14-18), translation and protection table (TPT) entries from a host memory for virtual to physical address translation (e.g., figure 4, element 450 , fig. 2A, memory 220 is a memory of the host system 200 and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65) and access validation to the host memory during I/O transactions(e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68), each of the TPT entries corresponds to a memory portion of the host memory (e.g. col. 2, lines 14-22 and col.1, lines 64-68; col. 3, lines 28-33 and col. 6, lines 55-60) and comprise at least a translation cacheable flag (e.g., col. 6, lines 5-45; col. 4, lines 35-40; col. 8, lines 24-45) and a memory protection tag to specify whether the adapter has permission to access the host memory (i.e. a memory protection label; e.g., col. 4, lines 35-45, col. 7, lines 55-65; col. 1, lines 49-55) and

Checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter to determine whether to discard one or more selected TPT entries from the cache of the adapter (e.g., col. 6, lines 5-45; col. 4, lines 35-40).

As per claim 26, Watkins shows an adapter in a host system (e.g., fig. 3, el. 260k is an adapter which joins a switch to bus 270, fig.2A, a workstation 200 is a host system because it is a computer connected to a network or work station 200,CPU 210 controls the attached peripheral devices 260, col. 3, lines 34-38 and col. 4, lines 50-60) provided to interface a switched fabric (e.g., fig. 3, an ATM Switch and network; col. 3, lines 14-18), comprising:

a cache memory (i.e., a memory in which frequently used data values being duplicated for quick access) for storing a set of translation and protection table entries from a host memory (e.g., figure 4, element 450, fig. 2A, memory 220 is a memory of the host system 200; and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65) for virtual to physical address translations and access validation to the host memory during I/O (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68), each of the TPT entries corresponds to a memory portion of the memory (e.g. col. 2, lines 14-22 and col.1, lines 64-68; col. 3, lines 28-33 and col. 6, lines 55-60) and comprises at least a translation cacheable flag (e.g., col. 6, lines 5-45; col. 8, lines 24-45); and a mechanism to determine a status of the translation cacheable flag of one or more selected TPT entries stored in the cache of the adapter (e.g., col. 6, lines 5-45; col. 4, lines 35-40; col. 8, lines 24-45) and a memory protection tag to specify whether the adapter has permission to access the host memory (i.e. a memory protection label; e.g., col. 4, lines 35-45, col. 7, lines 55-65; col. 1, lines 49-55) and

a mechanism to determine a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache (e.g., col. 6, lines 5-45; col. 4, lines 35-40; col. 8, lines 24-45, abstract), and to discard one or more selected TPT entries from the cache on the status of the translation of the cacheable flag (e.g., col. 6, lines 5-45; col. 4, lines 35-40; col. 8, lines 24-45, abstract).

As per claims 23 and 28, Watkins shows each of the selected translation and protection table entries represents translation of a single page of the host memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60).

6. Claims 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshioka et al., U.S. patent No. 5,835,963 (hereinafter Yoshioka).

As per claim 16, Yoshioka shows an apparatus, comprising:

a storage device to store translation table and protection table (TPT) entries for virtual to physical address translations (e.g., fig. 4, TLB entry, col. 10, line 35 to col. 11, line 3), wherein each of said TPT include protection attributes to control read and write access to a given memory region of a host memory (i.e., fig. 13, MPU or CPU is a host because it control the attached peripheral devices and MMRY is a main memory of the host or a cache memory is the memory of the host; e.g., fig. 30, TLB protection exception, col. 31, line 35 to col. 32, lines 5; col. 10, line 35 to col. 11, line 3), and a memory protection tag to specify whether said apparatus has permission to access said host memory (e.g., col. 21, line 45 to 6; col. 23, lines 10-30, col. 27, lines 20-55; col. 31, line 35 to col. 32, line 6); and a mechanism to flush individual TPT entries stored in the

storage device in accordance with a corresponding translation cacheable flag included in the individual TPT (e.g., fig. 4, V, fig. 8, col.28, lines 10-18; col. 24, lines 40-45).

As per claims 17-19, Yoshioka shows the storage device corresponds to an internal cache for storing said TPT entries (e.g., fig. 13, TLB, cache; col. 10, lines 40-45); each of the selected translation and protection table entries represents translation of a single page of the host memory (e.g. col. 10, lines 50-55); and each TPT entry comprising a physical page address field to address a physical page frame of data entry (e.g. col. 10, lines 50-55) and said translation cacheable flag to specify whether said apparatus may flush a corresponding translation and protection table (TPT) entry stored in said internal cache (e.g. col. 10, lines 35-55).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (5,937,436), in view of Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann)

As per claims 22 and 27, Watkins teaches the use of the adapter and TPT entry as discussed above. Watkins does not explicitly show the use an operating system to set the status of the translation cacheable flag per TPT entry for enabling to discard

individual TPT entries from the cache. Horstmann shows the use of an operating system to set the status of the translation cacheable flag per table entry for enabling to discard individual table entries from the cache (e.g. col. 11, lines 25; col. 1, lines 17-19 and col. 1, lines 49-55; col. 10, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann into the system of Watkins because it would increase translation speed from limiting number of reloading currently used data, reduce chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49.

9. Claims 1-14 are allowable over the prior art of record.

10. Claims 24-25 and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Applicant's arguments filed 3/27/06 have been fully considered but they are not persuasive.

12. In the remarks, the applicant argued that Watkins does not disclose a memory protection tag to specify whether said host fabric adapter has permission to access a host memory.

The examiner disagreed with the applicant's argument because Watkins teaches a host system (e.g., fig.2A, a workstation 200 is a host system because it is a computer connected to a network or work station 200,CPU 210 controls the attached peripheral devices 260, col. 3, lines 34-38 and col. 4, lines 50-60); and a memory protection tag to specify whether the adapter has permission to access the host memory (i.e. a memory protection label; e.g., col. 4, lines 35-45, col. 7, lines 55-65; col. 1, lines 49-55). According to the cited sections, the translated physical address is not output when an attempted write access of a read only page and the system cannot access the host memory if there is no translated physical address.

13. Applicant's arguments with respect to the other arguments have been considered but are moot in view of the new ground(s) of rejection.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday from 8:45 a.m. to 5:15 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D.T.
6/12/06